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10/015,434	12/13/2001	Bradley J. Howard	97-0008.01	7606

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Richard D. Egan
O'KEEFE, EGAN & PETERMAN
Building C, Suite 200
1101 Capital of Texas Highway South
Austin, TX 78746

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/015,434	HOWARD, BRADLEY J.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8-10,19,21-23,34-37 and 49-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8-10,19,21-23,34-37 and 49-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6, 8-10, 19 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agostino et al. (U.S. Patent 5,215,861) in view of Parikh (U.S. Patent 6,127,263).

In re claim 6, **Agostino** discloses a semiconductor device formed using a photo-definable layer **2** (organosilicon resist such as organosilane) (col. 2, lines 4-10) in a positive mask scheme (col. 4, lines 3-22 and FIG. 1),

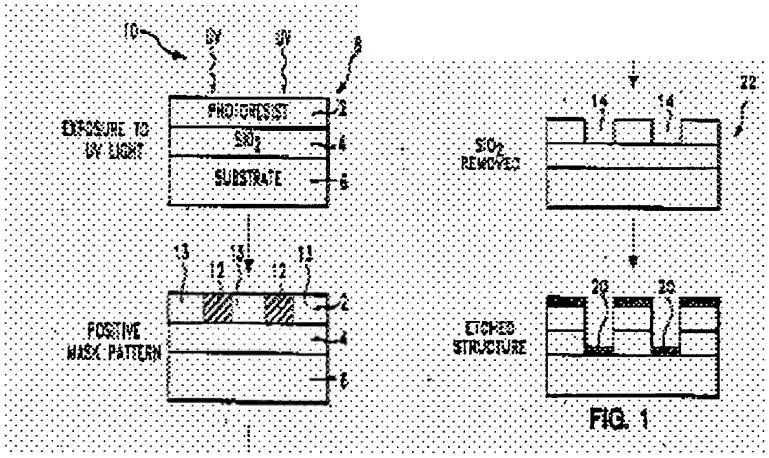


FIG. 1

comprising: a substrate **6**; at least one feature **14** formed on the substrate **6** by converting selected portion of a photo-definable layer **2** to an insulative material through exposure to electro-magnetic radiation **10** in a positive mask scheme and by using non-exposed portions **13** of the photo-definable layer **2** as a mask to form at least one feature

14; and an insulative layer formed on the substrate **6** from the non-exposed portion **13** of the photo-definable layer **2** which (1) remain after the positive mask scheme completes all masking steps that form the at least one feature **14** (col. 4, lines 3-22 and FIG. 1).

Agostino does not explicitly disclose the step of (2) subsequently converted to the insulative layer through exposure to further electro-magnetic radiation as recited in independent claim 6.

Parikh, however, teaches a semiconductor device formed using a photo-definable layer **418** (plasma polymerized methysilane (PPMS)) (col. 9, lines 33-38 and FIG. 4C), comprising:

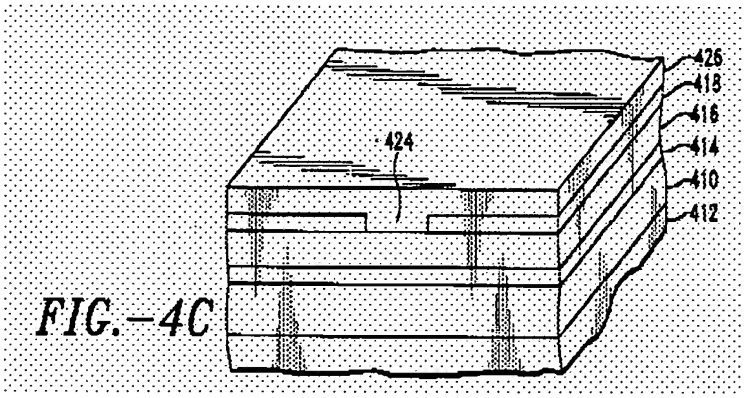


FIG.-4C

a substrate **412**; at least one feature **424** formed on the substrate **412** by (2) converting selected portions of a photo-definable layer **418** to an insulative material (plasma polymerized methylsilane oxide) (PPMSO)) (col. 9, lines 38-45) through exposure to further electro-magnetic radiation (col. 9, lines 27-50 and FIG. 4C).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Agostino and Parikh to enable the converted insulative layer of Agostino to be formed and furthermore to obtain an

improved methods for dual damascene fabrication to compensate for misalignment between the via mask and the trench mask (col. 2, lines 48-55, Parikh).

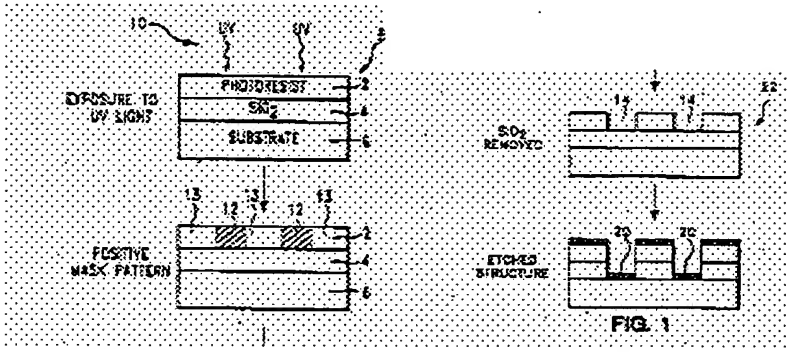
In re claim 8, as applied to claim 6 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the photo-definable layer 2 comprises an organosilicon resist such as organosilane (col. 2, lines 4-10, Agostino).

In re claim 9, as applied to claim 8 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the photo-definable layer 418 comprises plasma polymerized methylsilane (PPMS) (col. 9, lines 34-45, Parikh).

In re claim 10, as applied to claim 9 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the feature is part of a memory cell array (col. 1, lines 5-28, Parikh).

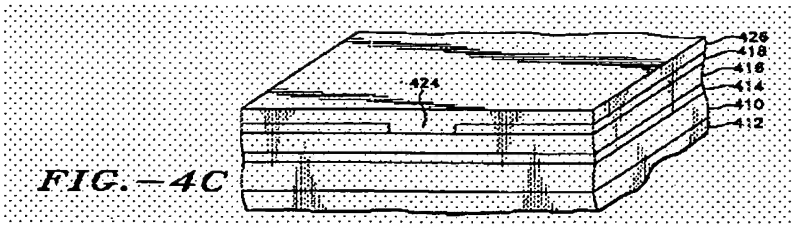
In re claim 19, **Agostino** discloses a patterned insulative structure within a semiconductor device formed using a photo-definable layer **2** (organosilicon resist such as organosilane) (col. 2, lines 4-10) in a positive mask scheme (col. 4, lines 3-22 and FIG. 1), comprising: a substrate **6**; and a patterned insulative layer formed on the substrate 6 in a positive mask scheme and by using non-exposed portions **13** of the photo-definable layer **2** as a mask to form the patterned insulative layer wherein the insulative layer comprises an oxide layer and the non-exposed portions of the photo-definable are utilized to mask the oxide layer to form the patterned insulative layer, wherein the patterned insulative layer comprises non-exposed portions of the photo-definable layer that were

converted into additional insulative material after formation of the patterned insulative layer (col. 4, lines 3-22 and FIG. 1).



Agostino does not explicitly disclose the step of converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation as recited in independent claim 19.

Parikh, however, teaches a semiconductor device formed using a photo-definable layer **418** (plasma polymerized methysilane (PPMS)) (col. 9, lines 33-38), comprising: a substrate **412**; at least one feature **424** formed on the substrate **412** by converting selected portions of a photo-definable layer **418** to an insulative material (plasma polymerized methylsilane oxide) (PPMSO)) (col. 9, lines 38-45) through exposure to further electro-magnetic radiation (col. 9, lines 27-50 and FIG. 4C).



Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Agostino and Parikh to enable the converted insulative layer of Agostino to be formed and furthermore to obtain an

improved methods for dual damascene fabrication to compensate for misalignment between the via mask and the trench mask (col. 2, lines 48-55, Parikh).

In re claim 21, as applied to claim 19 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the photo-definable layer **2** comprises an organosilicon resist such as organosilane (col. 2, lines 4-10, Agostino).

In re claim 22, as applied to claim 21 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the photo-definable layer 418 comprises plasma polymerized methylsilane (PPMS) (col. 9, lines 34-45, Parikh).

In re claim 23, as applied to claim 22 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the insulative layer comprises a plurality of trench structures (dual damascene structure) within a memory cell array (col. 1, lines 5-28, Parikh).

3. Claims 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh (U.S. Patent 6,127,263) in view of Agostino et al. (U.S. Patent 5,215,861).

In re claim 34, **Parikh** discloses a conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate **212** (col. 5, lines 10-16 and FIG. 2A);

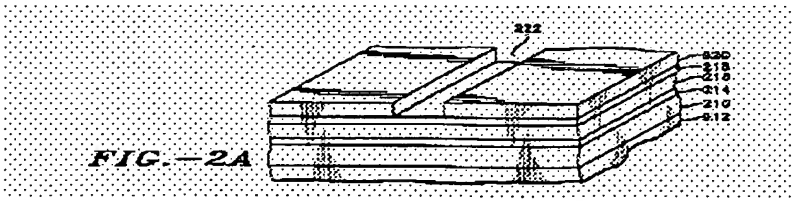


FIG.—2A

a first conductive layer over the substrate **212** (col. 5, lines 10-16);

an insulative layer **210** over the conductive layer; and

a second conductive layer **242** formed within a desired portion of the insulative layer **210** (col. 6, lines 27-36 and FIG. 2I) to create a conductive interconnect structure connected to the first conductive layer (col. 6, line 36), the second conductive layer **242** being formed within the desired portion of the insulative layer, the desired portion of the insulative layer being a void formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a mask scheme by using portions of the photo-definable layer as a mask to form a pattern within the insulative layer (col. 9, lines 34-45), and by using portions of the photo-definable layer as a sacrificial mask in etching the first conductive layer (col. 9, lines 45-50).

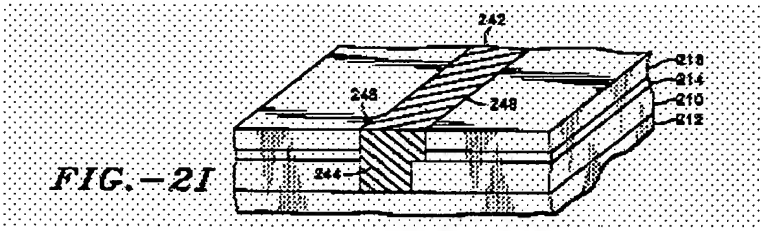


FIG.–21

Parikh, does not explicitly discloses converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme by using non-exposed portions of the photo-definable layer as a mask to form a pattern within the insulative layer as recited in present independent claim 34.

Agostino, however, discloses a semiconductor device formed using a photo-definable layer **2** (organosilicon resist such as organosilane) (col. 2, lines 4-10) in a positive mask scheme (col. 4, lines 3-22 and FIG. 1), comprising: a substrate **6**; at least

one feature **14** formed on the substrate **6** by converting selected portion of a photo-definable layer **2** to an insulative material through exposure to electro-magnetic radiation **10** in a positive mask scheme and by using non-exposed portions **13** of the photo-definable layer **2** as a mask to form at least one feature **14** within the insulative layer **2** (col. 4, lines 3-22 and FIG. 1).

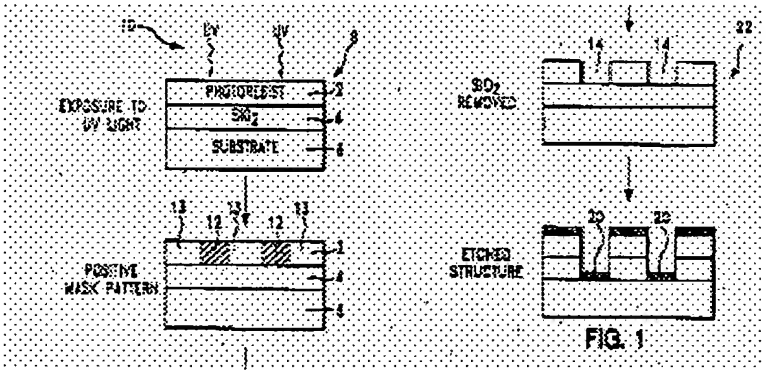


FIG. 1

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Parikh and Agostino to enable the converted insulative layer formed through exposure to electro-magnetic radiation in a positive mask scheme of Parikh to be formed and furthermore to provide a photosensitive material that may be used to formulate a photoresist material that is easily converted from a positive tone pattern to a negative tone pattern (col. 1, lines 43-47, Agostino et al.).

In re claim 35, as applied to claim 34 above, Parikh in combination with Agostino discloses all claimed limitations including the limitation wherein the photo-definable layer **2** comprises an organosilicon resist such as organosilane (col. 2, lines 4-10, Agostino).

In re claim 36, as applied to claim 35 above, Parikh in combination with Agostino discloses all claimed limitations including the limitation wherein the photo-definable

layer 418 comprises plasma polymerized methylsilane (PPMS) (col. 9, lines 34-45, Parikh).

In re claim 37, as applied to claim 34 above, Parikh in combination with Agostino discloses all claimed limitations including the limitation wherein the substrate includes a plurality of transistor gate structures for a memory cell array (col. 1, lines 5-28, Parikh).

4. Claims 49-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agostino et al. (U.S. Patent 5,215,861) in view of Parikh (U.S. Patent 6,127,263).

In re claim 49, **Agostino** discloses a patterned insulative structure within a semiconductor device using a photo-definable layer **2** (organosilicon resist such as organosilane) (col. 2, lines 4-10) as a mask layer, comprising: a substrate **6**; and an insulative layer on the substrate **6** in a positive mask scheme (col. 4, lines 3-22 and FIG. 1) and by using non-exposed portions **13** of the photo-definable layer **2** as a mask to form a pattern within the insulative layer, wherein the insulative layer comprises non-exposed portions of the photo-definable layer subsequently converted into additional insulative material (col. 4, lines 3-22 and FIG. 1).

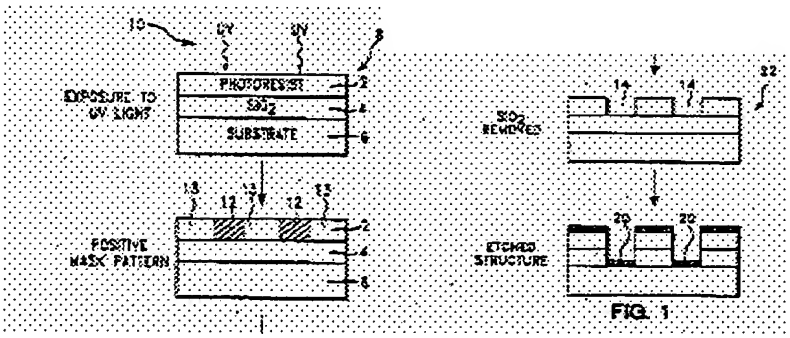


FIG. 1

Agostino does not explicitly disclose that the insulative layer on the substrate formed by covering a photo-definable layer with a separate patterned organic photoresist,

by converting unmasked portions of a photo-definable layer to an insulative material through exposure to electrode-magnetic radiation as recited in independent claim 49.

Parikh, however, teaches a semiconductor device having an insulative layer on the substrate **412** by covering a photo-definable layer **418** (plasma polymerized methysilane (PPMS)) (col. 9, lines 33-38) with a separate patterned organic photoresist **426** by converting selected portions of a photo-definable layer **418** to an insulative material (plasma polymerized methylsilane oxide) (PPMSO)) (col. 9, lines 38-45) through exposure to electro-magnetic radiation (col. 9, lines 27-50 and FIG. 4C).

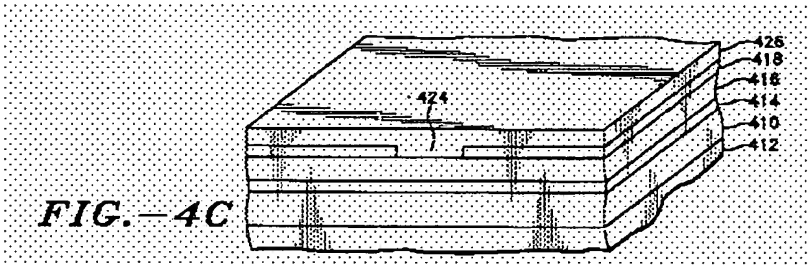


FIG.—4C

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Agostino and Parikh to enable the converted insulative layer of Agostino to be formed and furthermore to obtain an improved methods for dual damascene fabrication to compensate for misalignment between the via mask and the trench mask (col. 2, lines 48-55, Parikh).

In re claim 50, as applied to claim 49 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the photo-definable layer **2** comprises an organosilicon resist such as organosilane (col. 2, lines 4-10, Agostino).

In re claim 51, as applied to claim 50 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the photo-definable layer **418** comprises plasma polymerized methylsilane (PPMS) (col. 9, lines 34-45, Parikh).

In re claim 52, as applied to claim 51 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the insulative layer comprises an oxide layer (plasma polymerized methylsilane oxide (PPMSO)) (col. 9, lines 38-41, Parikh).

In re claim 53, as applied to claim 52 above, Agostino in combination with Parikh discloses all claimed limitations including the limitation wherein the insulative layer comprises a plurality of trench structures (dual damascene structure) within a memory cell array (col. 1, lines 5-28, Parikh).

Response to Applicant's Amendment and Argument

5. Applicant's arguments filed October 10th, 2006 have been fully considered but they are not persuasive.

Applicant contend that the references Agostino et al. (U.S. Patent 5,215,861), herein known as Agostino, in view of Parikh (U.S. Patent 6,127,263), herein known as Parikh does not teach or suggest a second subsequent exposure after the first masking exposure is performed to convert that originally non-exposed portion of PPMS of Parikh to an insulative layer.

In response to Applicant's contention that Agostino in view of Parikh does not teach or suggest subsequently converted to the insulative layer through exposure to further electro-magnetic radiation, Examiner respectfully disagrees.

Applicant's attention is directed to (col. 4, lines 3-22 and FIG. 1), where Agostino discloses a substrate 6, at least one feature 14 formed on the substrate 6 through exposure to electro-magnetic radiation (UV) in a positive mask scheme and by using non-exposed portions 13 of the photo-definable layer 2 (photoresist) as a mask to form the at least one feature 14. Agostino does not explicitly shows subsequent step of converting the photo-definable layer which (1) remain after the positive mask scheme to the insulative layer through exposure to further electro-magnetic radiation. The secondary reference, Parikh, however, suggests that a photo-definable layer (CVD plasma polymerized methylsilane, PPMS) 418 being used as a mask to form a feature (trench pattern) 424 capable of exposed to further electro-magnetic radiation (UV light) to convert into plasma polymerized methylsilane oxide (PPMSO) (col. 9, lines 33-50 and FIG. 4B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Parikh into Agostino to use the PPMS layer of Parikh as a mask to form a feature, and then expose the PPMS layer to further electro-magnetic radiation to convert the PPMS layer to PPMSO layer for further processing.

For this reason, Examiner holds the rejection proper.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
January 20, 2007

Brook Kebede
BROOK KEBEDE
PRIMARY EXAMINER